ABSTRACT OF THE DISCLOSURE

The present invention provides a low-voltage-triggered electrostatic discharge (LVTESD) protection circuit coupled to a pad of an integrated circuit (IC) to protect core circuits of the IC from ESD. The ESD protection circuit comprises a semiconductor substrate having the first conductivity type, a well region having the second conductivity type is formed in the semiconductor substrate, and an anode-doped region having the first conductivity type and formed in the well region to become an anode of a semiconductor control rectifier (SCR). A gate structure is formed in the semiconductor substrate outside the well region. A first doped region having the second conductivity type is formed between the well region and the gate structure in the semiconductor substrate. A second doped region having the second conductivity type is formed adjacent to the second side of the gate structure in the semiconductor substrate. A plurality of isolated islands are evenly formed and distributed in the first doped region so that current in the first doped region must flow around the isolated islands to increase the resistance of the first doped region.